Notice of Allowability	Application No.	Applicant(s)	
	10/802,894	MORAVEJI, FARHOOD	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Tel. Int. 03/17/05*.

2. ☒ The allowed claim(s) is/are *1-25*.

3. ☒ The drawings filed on *16 March 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 5/7/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *3/17/05* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

MY-TRANG NU TON
PRIMARY EXAMINER
3/17/05

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Att. Bever on March 17, 2005.

The application has been amended as follows:

In claim 9, line 10, replace "first" with – second --.

In claim 21, line 1, replace "22" with – 20 --.

Reasons for allowance

The following is an examiner's statement of reasons for allowance:

The present invention is drawn to an amplifier circuit utilizing first – second input terminals, first – second output terminals, first – second complementary metal-oxide-semiconductor inverters, first – second bias circuits (or means for regulating a first DC bias voltage, means for regulating a second DC bias voltage, or first - second operational amplifiers) recited in claims 1-25. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: "**the first bias circuit for applying linear biasing to the first CMOS inverter, the first bias circuit being coupled between an output of the first CMOS inverter and the input of the first CMOS inverter**" and "**the second bias circuit for applying linear biasing to the second CMOS inverter, the second bias**

circuit being coupled between an output of the second CMOS inverter and the input of the second CMOS inverter" in combination with "**the first complementary metal-oxide-semiconductor CMOS inverter**" and "**the second complementary metal-oxide-semiconductor CMOS inverter**" as recited in claim 1; "**applying linear biasing to the first CMOS inverter and the second CMOS inverter**" in combination with "**supplying a first alternating current (AC) signal to the input of the first CMOS inverter and a second AC signal to the input of the second CMOS inverter to generate an amplified differential signal**" as recited in claim 10; "**means for regulating a first DC bias voltage at an input of the first CMOS inverter to force a DC offset voltage at an output of the first CMOS inverter to a reference voltage between an upper supply voltage and a lower supply voltage**" in combination with "**means for regulating a second DC bias voltage at an input of the second CMOS inverter to force a DC offset voltage at an output of the second CMOS inverter to the reference voltage**" as recited in claim 17; "**the first operational amplifier ... coupled to an input of the first CMOS inverter**" in combination with "**the second op-amp ... coupled to an input of the second CMOS inverter**" as recited in claim 22.

The prior art references submitted by the applicant on IDS form received on 5/7/04 was reviewed and considered. These references appear to be the best references with respect to the claimed invention and closely matched most of the references found during the examiner's searches. However, as noted above, the limitation "the first - second bias circuits" (claim 1); the combination of all the method steps (claim 10), "means for regulating a first DC bias voltage" and "means for

regulating a second DC bias voltage" (claim 17); "the first op-amp" and "the second op-amp" (claim 22) are not disclosed. Therefore, the claims are patentably distinct over all these prior art references of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816

3/17/05